REMARKS/ARGUMENTS

In the most recent Office Action, claims 1-14 were pending. Claims 1-14 stand rejected.

In response, claims 1-14 remain pending in the present application. No new matter is added.

Applicant thanks the Examiner for the thorough search and examination of the present application, and responds to the comments in the Office Action as follows.

SPECIFICATION

The Abstract of the Disclosure is objected to for containing more than 150 words. In response, a new Abstract is submitted that complies with the requires for patent specifications. Entry is respectfully requested.

Applicant respectfully submits that the substitute Abstract overcomes the objection, and reconsideration and withdrawal of the objection is respectfully requested.

Claim Rejections - 35 U.S.C. §102

The Office Action states that claims 1-14 are rejected under 35 U.S.C. §102(b) as being anticipated by Wilhelm et al. (U.S. Patent No. 6, 211,623). In particular, the Office Action states that Wilhelm et al. discloses each and every element recited in claims 1-14. Applicant respectfully traverses the rejection.

The disclosure by Wilhelm et al. teaches an electronic ballast control for driving a half bridge at particular switching frequencies based on the selection of external components. The disclosure by Wilhelm et al. does not in any part discuss a power factor correction circuit, or power factor correction control, with the exception of a mere mention that PFC control may be used on a DC bus (col. 12, lines 50-53).

Altogether missing from the discussion provided by Wilhelm et al. is any mention or indication of power factor circuitry in an integrated circuit. Claims 1-7 recite an integrated circuit with:

power factor control circuitry coupled to the ballast control circuitry and operable to regulate ballast power to obtain an improved power factor correction for the ballast.

Claims 8 and 9 recite a number of elements that are completely absent from the disclosure by Wilhelm et al., including:

sensing a zero crossing on an input voltage;

increasing a switch on time as the input voltage approaches the zero crossing to provide for power factor correction with reduced crossover distortion;

increasing a gain of a power factor correction loop to obtain a fast response;

reducing a gain of a power factor correction loop to optimize ballast power factor; and

controlling an inductor by activating a switch in a boost-type power factor correction circuit.

Wilhelm et al. fail to disclose any of these elements because the ballast control by Wilhelm et al. fails to disclose any type of power factor correction methods.

Claims 10 and 12 recite a control circuit with a number of states, including:

a preheat control state for switching a half bridge in the electronic ballast at a first frequency and providing power factor correction with a fast response time; and

a run control state with the power factor correction operating in low gain with optimized power factor correction.

Once again, Wilhelm et al. has a complete lack of disclosure with respect to a power factor control or circuitry for accomplishing power factor correction.

Claim 11 recites a power factor correction circuit integrated in an electronic ballast, including:

> an inductor current sensing section for detecting a zero current crossing of an inductor;
>
> a variable gain control section coupled to the input voltage sensing section and operable to provide variable close loop feedback gain in the power factor correction circuit;
>
> a compensation indication coupled to the variable gain control section for influencing a closed loop gain of the variable gain control section; and
>
> an output section coupled to the variable gain control section and the inductor sensing section for driving a power factor correction switch, an on time of the output section being related to the input voltage, the closed loop gain and the zero current crossing.

These features recited in claims 11 and 13 are not disclosed anywhere in the cited reference by Wilhelm et al.

Turning to claim 14, a single chip integrated ballast control is recited including:

> a power factor correction circuit coupled to the control circuit and operable to control input power to improve a ballast power factor.

Wilhelm et al. fail to teach any type of power factor correction circuit integrated into a single chip with a half bridge driver and a control circuit for a ballast.

The present invention recited in claims 1-14 provides a number of novel features that are not disclosed in any of the cited prior art references, including an integrated power factor correction control circuit on the same chip as a ballast control. This advance in electronic ballast controls represent a significant departure from prior art systems and obtains a number of advantages including reduced component count, reducing cost and reduced complexity. Applicant has recited in claims 1-14 a number of elements that are not taught in the disclosure by

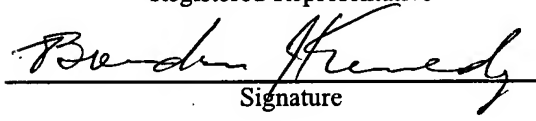
Wilhelm et al. Accordingly, because the limitations recited in claims 1-14 are not all taught in the disclosure by Wilhelm et al., the rejection under 35 U.S.C. §102(b) cannot be maintained against those claims. Applicant respectfully requests that the rejection of claims 1-14 under 35 U.S.C. §102(b) be reconsidered and withdrawn.

Conclusion

Applicant has carefully studied the other prior art references of record and believes that the claims in the application patentably distinguish over those references. In view of the above comments, applicant respectfully submits that the application is now in condition for allowance, and earnestly solicits notice to that effect. If it is believed that an interview would contribute to progress in the application, the Examiner is requested to contact the undersigned counsel at the number provided below.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 7, 2004:

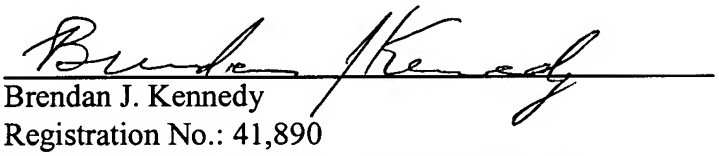
Brendan J. Kennedy
Name of applicant, assignee or Registered Representative



Signature

September 7, 2004
Date of Signature

Respectfully submitted,



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